Analysis and Improvement of Intermodulation Distortion in GaAs Power FET's

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Abstract—**Tailoring of the doping profile is a powerful tool in reducing the intermodulation distortion (IMD) in GaAs power FET's. Reproducible and uniform preparation of the required profiles is a difficult task for epitaxial techniques. This shortcoming has motivated the present investigation of fabricating highly linear power FET's by ion implantation. An analytical device model was developed for exploring the relationship between the active layer profile and the IMD. These calculations revealed a complex behavior in the variation of the distortion levels due to partial correlation between the contributions arising from nonlinear transconductance and output conductance. The device model was used to identify implant doses and energies for approaching an optimum active layer profile. Based on the results, a deep Se implant followed by a shallow compensating Be implant to reduce the doping level close to the surface was used in the device fabrication. The IMD of the transistors was measured by the two-tone method. Conventional epitaxial FET's with a flat doping profile were evaluated for comparison purposes. This comparison demonstrated that a 4-dB increase in the intercept point for the third-order intermodulation product can be realized by using the tailored implanted profile. The experiments demonstrated that the tuning conditions for maximum output power and minimum IMD are virtually identical for the implanted transistors, in contrast to the behavior of conventional devices with flat doping profiles. These performance advantages, coupled with the high levels of uniformity and reproducibility of doping parameters, show ion implantation to be a powerful technique in the fabrication of highly linear power FET's.**

List of Symbols

A	Amplitude of signal at frequency f_1
B	Amplitude of signal at frequency f_2
Be^+	Beryllium implantation
$C_d(V)$	Drain-to-source capacitance
$C_g(V)$	Gate-to-source capacitance
C_{gn}	Polynomial coefficient of gate capacitance for the nth power
f_1, f_2	Two RF frequencies simultaneously applied to the amplifying device
$G_m(V)$	Device transconductance
$G_d(V)$	Device drain conductance
G_{mn}	nth power polynomial coefficient of transconductance
G_{dn}	nth power polynomial coefficient of drain conductance
$I_g(t)$	RF current in the gate
$I_d(t)$	Device RF drain current
I_{f_1}	Device drain current at f_1
$I_{mf_1 \pm nf_2}$	Device drain current at $mf_1 \pm nf_2$
$I'_{mf_1 \pm nf_2}$	Device drain current at $mf_1 \pm nf_2$ due to transconductance distortion
$I''_{mf_1 \pm nf_2}$	Device drain current at $mf_1 \pm nf_2$ due to drain side distortion
L_L	Load tuning inductance
L_g	Gate tuning inductance
Q_g	Charge on the gate capacitance
R_s	Signal source resistance
R_L	Load resistance
Se^+	Selenium implantation
$V_{gs}(t)$	Instantaneous gate voltage
V_g	RF gate voltage
V_{g0}	Gate bias voltage
V_d	RF drain voltage
V_{d0}	Drain bias voltage
$V_{ds}(t)$	Instantaneous drain voltage
Y_L	Complex load admittance.

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I. Introduction

THE GaAs field effect transistor has emerged as a highly attractive device in power amplifier applications through the demonstration of multiwatt power output levels at X-band frequencies with power added efficiencies of up to 40 percent. Initial explorations in the design of linear amplifiers have shown that the behavior of nonlinear distortion, characterized by third-order intermodulation distortion (IMD) levels, is complex and needs to be better understood by both the device designer and the systems user [1]–[3]. Williams and Shaw [4] suggest the use of "graded" profiles to improve the IMD behavior of GaAs FET's and accompany this suggestion with supporting experimental results. The present work is aimed at providing a more complete understanding of the sources of IMD in a FET by studying their relationship to various doping profiles, and of how a better profile with respect to improved linearity may be obtained by ion implantation.

Implantation offers considerable flexibility in profile tailoring by employing multiple implant energies, doses, and doping species. Calculations of theoretical profiles were carried out and used in conjunction with device modeling and distortion analysis in order to identify improved implant profiles for linear power FET's. These

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calculations are discussed in Section II and show that a deep Se implant with a subsequent shallow compensating Be implant of moderate dose can furnish active layers for power FET's with highly linear characteristics. The calculations verify the complex nature of the distortion in GaAs FET's in that dips in the IMD levels as a function of input power can be predicted and explained.

A brief outline of the device fabrication is presented in Section III, including doping profiles resulting from combined Se+Be implants. The contact deposition and pattern definition essentially follow the technology established for fabricating low-noise FET's [5].

RF measurement procedures and results are discussed in Section IV. The main conclusions of the device modeling are confirmed by the measured results. A 4-dB improvement in the intercept point for the third-order intermodulation product was achieved from a Se+Be implanted FET compared to a conventional device employing a flat doping profile. Also, the strong correlation in the sources of nonlinearity was confirmed by the observations of sharp dips in the third- and higher order intermodulation products as functions of the input power.

II. IMD

A. Device Modeling

The simplified equivalent circuit of a tuned GaAs power FET amplifier (Fig. 1) will be used to highlight the primary sources of nonlinear behavior. The nonlinearities in the FET can be accounted for by introducing appropriate variations in the equivalent circuit elements as functions of the instantaneous drain and gate voltages. A good approximation of these functional dependencies can be obtained from static calculations. Such calculations show that the dominant contributions to nonlinear response can be expected from the variation in transconductance G_m with gate voltage and in the drain conductance G_d with drain voltage. Additional contributions arise from the voltage dependence of the gate-source capacitance C_g. It will be assumed that the static capacitance between the source and the drain is much larger than the variable contribution, so that the drain capacitance may be assumed to contribute very little IMD.

Mathematically, it is convenient to represent the variation in the equivalent circuit elements in a Taylor series around the operating point. By this approach, the transconductance can be written

$$G_m(V) = G_{m1} + G_{m2}V_g + G_{m3}V_g^2 + G_{m4}V_g^3 + \cdots \quad (1)$$

and therefore, the device RF drain current would be given by the terms

$$I_d(t) = \int_0^{V_g(t)} G_m(V)\,dV = G_{m1}V_g + G_{m2}\frac{V_g^2}{2} + G_{m3}\frac{V_g^3}{3} + G_{m4}\frac{V_g^4}{4} + \cdots \quad (2)$$

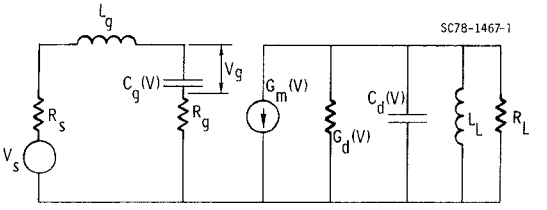

Fig. 1. Equivalent circuit of a power FET in a tuned amplifier.

where

$$V_g = V_{gs}(t) - V_{g0} \quad (3)$$

specifies the instantaneous deviation of the gate-source voltage from the gate bias V_{g0}. In determining the expansion coefficients G_{mn}, a polynomial fit is made to the calculated variation in the transconductance from a forward gate voltage of 0.5 V to a reverse voltage corresponding to pinchoff. The variation in G_m with drain bias is neglected by averaging this variation over the typical range of drain voltages.

A corresponding expression can be written for the drain output conductance as a function of the drain voltage

$$G_d(V) = G_{d1} + G_{d2}V_d + G_{d3}V_d^2 + G_{d4}V_d^3 + \cdots \quad (4)$$

where

$$V_d = V_{ds}(t) - V_{d0} \quad (5)$$

represents the instantaneous deviation in the drain voltage from the bias voltage V_{d0}. The dependence of G_d on gate bias has been neglected by averaging this variation over the gate voltage range. The drain voltage range used in the calculation of the expansion coefficients extends from half of the saturation voltage to twice the drain bias voltage.

An analogous expression to (1) and (4) expresses the capacitance C_g as a function of the instantaneous signal voltage $V_g(t)$:

$$C_g(V) = C_{g1} + C_{g2}V_g + C_{g3}V_g^2 + C_{g4}V_g^3 \cdots \quad (6)$$

The effective impedance of this capacitance is derived from the equation

$$I_g(t) = \frac{d}{dt}[Q_g] = \frac{d}{dt}\left[\int_0^{V_g(t)} C_g(V)\cdot dV\right] \quad (7)$$

and from this relationship the IMD current levels due to the nonlinearity of $C_g(V)$ can be derived. However, the distortion due to this source is generally found to be small. Therefore, the main effect of the capacitance variation with voltage is seen to be a detuning effect with increasing signal drive level which gives rise to the sometimes observed gain expansion effects.

The expansion coefficients of $C_g(V)$ are derived from static calculations. As expected, calculations show that all the expansion coefficients such as G_{mn}, G_{dn}, and C_{gn} are dependent on the doping profile of the active layer. These coefficients can be used in turn to calculate IMD products using the methods of Tucker and Rauscher [6].

B. Carrier Profile Modeling

Practically all modeling of GaAs FET's has used analytical expressions derived from Shockley's [7] early work.

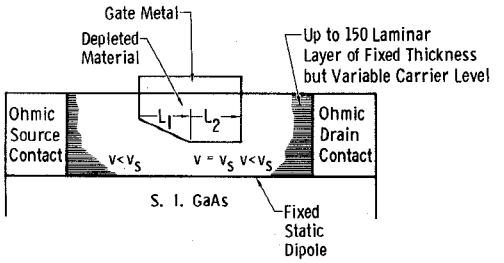

Fig. 2. Laminar layer models used in the modeling of GaAs FET's with variable carrier concentration profiles.

Pucel *et al.* [8] in a more detailed model have included the effects of velocity saturation. These analyses of FET devices depended upon the assumption of a flat profile of a certain thickness for purposes of simplification. To achieve the ability to deal with arbitrary profiles, numerical integration techniques have been adapted to the Pucel model.

Fig. 2 represents the model used to calculate the effects of nonflat profiles. The model deals with an arbitrary profile by dividing up the thickness of the active layer into 150 laminar layers. The passage of an electron under the gate region is modeled as having a region of saturated velocity following the initial short section where velocity is proportional to electric field. By observing the necessary boundary conditions in the directions along and normal to the charge flow, current may be established as a function of bias conditions. Also, gate capacitance, transconductance, and output conductance may be calculated over any range of bias conditions.

The computer is programmed to accept an analytical description of an active layer profile and to provide data on devices of specified geometry. The polynomial expansion coefficients describing G_m, C_g, and G_d over specified ranges of bias V_g and V_d are obtained from the computer.

C. Comparison of Implanted and Epitaxial Profiles

The most common technique for preparing GaAs FET active layers is vapor phase epitaxy. This approach offers some flexibility with regard to carrier profile tailoring [4], and has provided power FET's with outstanding performance. Therefore, it is of interest to compare the theoretical performance of FET's with implanted and epitaxial profiles in order to assess whether the intrinsic advantage of ion implantation in terms of reproducibility and uniformity can be effectively utilized in the fabrication of highly linear transistors.

This type of assessment will be carried out by comparing the relative merits of an idealized epitaxial profile, as described by Williams and Shaw [4], with abrupt doping transition toward the substrate, and the profile resulting from a 500-keV Se implant compensated at the surface by a shallow 40-keV Be implant. These profiles are shown in Fig. 3 along with a conventional flat doping profile, which will serve as a reference for the predicted performance. The devices modeled for this comparison were 500-μm wide gates of 1-μm length with ohmic contact resistance of $10^{-6}\ \Omega\cdot\text{cm}^2$.

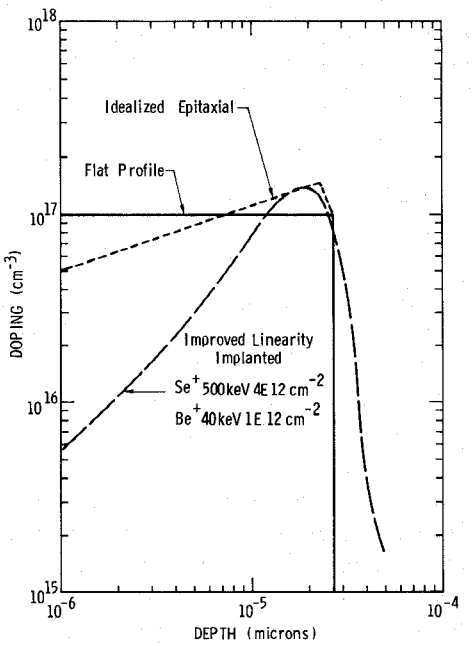

Fig. 3. Implanted and epitaxial doping profiles used in calculating the IMD characteristics of GaAs FET.

TABLE I
POLYNOMIAL COEFFICIENTS OF TRANSCONDUCTANCE
$G_m(V) = G_{m1} + G_{m2}V + G_{m3}V^2 + G_{m4}V^3 \cdots$

Coefficient	Flat Epi	Improved Epi	Ion Implant Se + Be
G_{m1}	0.035	0.0355	0.031
G_{m2}	0.0058	0.004	0.0033
G_{m3}	-0.00045	-0.0007	0.00075
G_{m4}	0.00033	0.00058	-0.000054
G_{m5}	0.00146	0.0009	-0.0002
G_{m6}	0.00005	-0.0001	0.000042
G_{m7}	-0.0002	-0.0001	0.0000448
G_{m8}	0.000005	0.000015	-0.0000047

TABLE II
POLYNOMIAL COEFFICIENTS OF DRAIN OUTPUT CONDUCTANCE
$V_{ds} = 10$ V, $G_d(V) = G_{d1} + G_{d2}V + G_{d3}V^2 + G_{d4}V^3 \cdots$

Coefficient	Flat Epi	Improved Epi	Ion Implant Se + Be
G_{d1}	1.64 E-4	1.99 E-4	4.28 E-4
G_{d2}	-3.07 E-5	-4.19 E-5	-4.90 E-5
G_{d3}	1.13 E-5	5.18 E-6	-2.23 E-6
G_{d4}	-1.37 E-6	7.62 E-7	1.23 E-7
G_{d5}	-3.92 E-7	-2.25 E-7	1.26 E-7
G_{d6}	5.80 E-8	-8.47 E-9	-2.02 E-8
G_{d7}	6.20 E-9	5.40 E-9	2.00 E-9
G_{d8}	-8.21 E-10	-3.41 E-10	-1.08 E-10

The modified Pucel model was used to derive the G_m and G_d polynomial coefficients for these three profiles. The results are shown in Tables I and II. It is important to note that the magnitude of the fifth-order (G_{m5}, G_{d5}) coefficients is least for the ion implanted profile, promising a better high power IMD performance. It is also noteworthy that in the case of transconductance, G_{m5} is larger than the G_{m3} coefficient for the flat profile device.

TABLE III
POLYNOMIAL COEFFICIENTS OF GATE-SOURCE CAPACITANCE (pF/V^{n-1}), $C_g(V)=C_{g1}+C_{g2}V_g+C_{g3}V^2+C_{g4}V^3\cdots$

Coefficient	Flat Epi	Ion Implant Se + Be
C_{g1}	0.2786	0.2482
C_{g2}	0.0467	0.0245
C_{g3}	0.0127	0.00029
C_{g4}	0.0004	0.0005
C_{g5}	-0.0016	-0.0003
C_{g6}	0.0025	0.0002
C_{g7}	0.0012	-0.00004
C_{g8}	-0.0008	-0.00004

The corresponding coefficients for the gate-source capacitance are given in Table III for the flat profile and the Se+Be implant. A comparison of the magnitude of the coefficients for each order reflects the smaller variation in this capacitance versus gate voltage for the implanted profile, which should reduce gain expansion effects and minimize IMD contributions from this source.

D. IMD

The calculated IMD is based on the normal two-tone method. The calculations assume that the IMD voltage levels are less than 10 percent of the voltage levels of the two carrier tones. This assumption restricts the range of validity of the calculated IMD levels to less than 20 dB below the carrier level. This ratio is quite adequate for analyzing linear amplifiers, as the operating point of interest will be below this level. In the calculations of signal power gain and IMD products, fixed values of R_s, the source resistance, and R_L, the load resistance, are used. The value of load resistance R_L is chosen to be 180 Ω rather than the value $(G_{d1})^{-1}$. This choice reflects the usual condition for large-signal tuning, where the output impedance of the device is much lower than $(G_{d1})^{-1}$. The load impedance presented at the harmonic bands, i.e., frequencies much higher than the signal frequency is assumed to be very small.

Only third-order products have been calculated. Normally, it is assumed that the third-order coefficient (G_{m3}, for instance) is much larger than the fifth- or seventh-order coefficients (G_{m5}, G_{m7}); from Table I this is evidently not so. From Tables I and II, it is seen that the fifth-order coefficients can contribute substantially to third-order IMD products. In fact, for moderate to high signal levels, the transconductance contributes mainly from its fifth-order (G_{m5}) term. This analysis contributes new insight into IMD generation by taking into account the contribution to third-order IMD products from the higher order terms in the nonlinear devices.

Tables IV and V give some indication of a) how the various coefficients contribute to the manner in which the conductance (and susceptance) levels change as the signal power level rises (Table IV), and b) how each expansion term adds to the various intermodulation frequencies (Table V). The implications of Table IV are that optimum

TABLE IV
THE (ω_1) CURRENT COMPONENTS RESULTING FROM DRIVING A NONLINEAR CONDUCTANCE $G(V)=G_1+G_2V+G_3V^3\cdots+$ WITH A TWO-TONE SIGNAL $V=A\cos\omega_1 t+B\cos\omega_2 t$, $I(t)=\int G(V)dV$

Source	Component	Component if B = 0
G_1V	A	A
$G_3V^{3\pm3}$	$0.25A^3+0.5A^2B$	$0.25A^3$
$G_5V^{5\pm3}$	$0.125A^5+0.75A^3B^2+0.375AB^4$	$0.125A^5$

TABLE V
THE CURRENTS CONTRIBUTED AT REPRESENTATIVE INTERMODULATION FREQUENCIES BY THE INDIVIDUAL COEFFICIENTS OF A NONLINEAR CONDUCTANCE $G(V)$ WHERE $I(t)=\int G(V)dV$ AND $G(V)=G_1+G_2V+G_3V^2\cdots$ AND $V=A\cos(\omega_1 t)+B\cos(\omega_2 t)$[a]

IMD Source	Two-Tone Test Intermodulation Products $2f_1-f_2$	$3f_1-2f_2$	$4f_1-3f_2$
$G_3V^{3\pm3}$	$0.25A^2B$		
$G_5V^{5\pm5}$	$0.25A^4B$	$0.125A^3B^2$	
	$0.375A^2B^3$		
$G_7V^{7\pm7}$	$0.234A^6B$	$0.234A^5B^2$	$0.078A^4B^3$
	$0.937A^4B^3$	$0.3127A^3B^4$	
	$0.468A^2B^5$		

[a] For $G_3\neq0$ $G_5\neq0$ $G_{n>5}=0$; $I_{2f_1-f_2}=0.25G_3A^2B+0.25G_5A^4B+0.375G_5A^2B^3$

tuning and loading conditions change with signal power level because of the corresponding changes in the admittance matrix of the device. The IMD levels would be sensitive to tuning and loading conditions because they depend upon the peak RF voltage levels. Therefore, different IMD performance may be expected for large-signal and small-signal tuning conditions.

Another point to be made is that in the low power signal region, the IMD contributions of the drain conductance $G_d(V)$ dominate; and, as the signal level rises, the $G_m(V)$ contributions to IMD products become larger. The intermodulation produced from the nonlinearities due to the transconductance and the output conductance can be expected to be partially correlated as a result of the coherence between the gate and the drain voltages. This correlation is commonly observed as a cancellation effect giving dips in the IMD versus input level curve. These dips are accompanied by a change in the rate of rise of the IMD power levels for a given increment of change in input power levels.

The sign of the fifth-order relative to the third-order coefficient may be quite important in determining the IMD products at low signal levels. In fact, cancellation effects can occur in third-order IMD products from the drain (or gate) alone due to sign differences of the different coefficients.

E. Profile Effects on IMD

The equivalent circuit in Fig. 1 has been used in conjunction with the information in Tables I to V to calculate

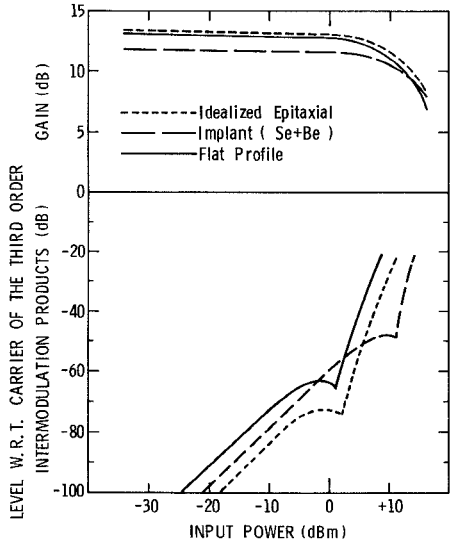

Fig. 4. Calculated gain and third-order intermodulation products versus input power using the active layer profiles in Fig. 3.

the gain and the third-order intermodulation products of the three profiles shown in Fig. 3. The results are given in Fig. 4.

It is observed that the gains at small-signal levels of both epitaxial devices are about 1 dB greater than the corresponding gain of the implanted transistor. This calculation is for a 10-GHz test where the signals (two tones) are separated by only a few MHz. The gain of the ion implanted device is less but saturates more slowly at high output power levels.

The IMD products display three distinct regions. At very low signal level, the third-order products rise 3 dB for a 1-dB increase in input signal level. This behavior is explained by the dominant role of G_{d3} in this range. Then comes the intermediate signal level region where the cancellation effects are generally seen. In the large-signal region, the contribution from the transconductance G_m generally dominates, and the rate of rise of the IMD product is greater than 3-dB/1-dB increase in signal level. This strong increase is caused by the large contribution from G_{m5} which may equal or exceed G_{m3}. Ion implantation shows a considerable advantage in this area because G_{m5} is much less than G_{m3} for this case and is lower than equivalent values for the other profiles; this results in the IMD product for the ion implanted FET continuing to have lower level with respect to the carrier up to higher input power levels. Thus the transition from drain side (G_d) dominated IMD to gate side dominated (G_m) IMD is postponed longer in the case of the implanted FET.

At the point of saturation, where output power is considerable and gain is falling to low values, the IMD products of the simple model become inaccurate. The rate of rise of the IMD products should fall off rather than continuing to rise at the higher rate shown in Fig. 4. The reason for this discrepancy is that the assumption of small IMD voltages becomes inaccurate and the total power is rapidly diverted into an increasing number of unwanted

TABLE VI

POLYNOMIAL COEFFICIENTS OF DRAIN CONDUCTANCE FOR DIFFERENT DRAIN BIAS CONDITIONS.

Coefficient	V_{ds} = 6V	V_{ds} = 10V
G_{d1}	3.32 E-4	4.28 E-4
G_{d2}	5.04 E-4	-4.90 E-5
G_{d3}	2.10 E-3	-2.23 E-6
G_{d4}	-6.47 E-4	1.23 E-7
G_{d5}	-5.12 E-4	1.26 E-7
G_{d6}	1.29 E-4	-2.02 E-8
G_{d7}	3.10 E-5	-2.00 E-9
G_{d8}	-7.00 E-6	-1.08 E-10

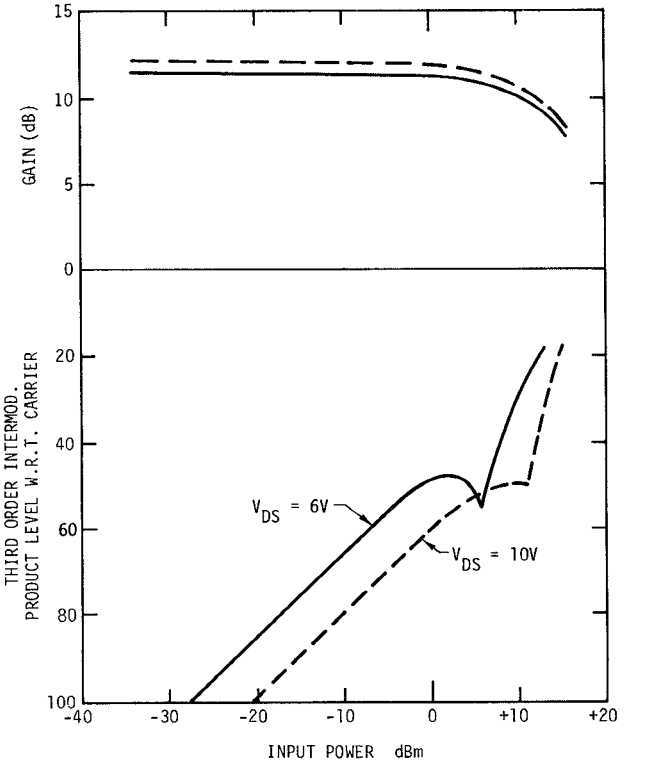

Fig. 5. Calculated gain and third-order intermodulation product versus input power for implanted GaAs FET with the drain voltage as a parameter.

IMD products other than just the third-order products. This area of the IMD versus input power level is tractable to computation using methods that a) account for many frequencies of nonnegligible voltage level, b) account for the total power distribution, and c) extend the power series representation for the equivalent circuit elements to a sufficiently high order.

F. Bias Dependence

The dependence of IMD on drain bias level has been calculated for the implanted profile in Fig. 3. The principal result of a rise of drain bias level is a general reduction of the G_d coefficients. This effect is illustrated by the results in Table VI, which lists the polynomial expansion coefficients of $G_d(V)$ for drain bias voltages of 6 and 10 V. The resulting IMD products have been calculated and are shown in Fig. 5. The IMD products

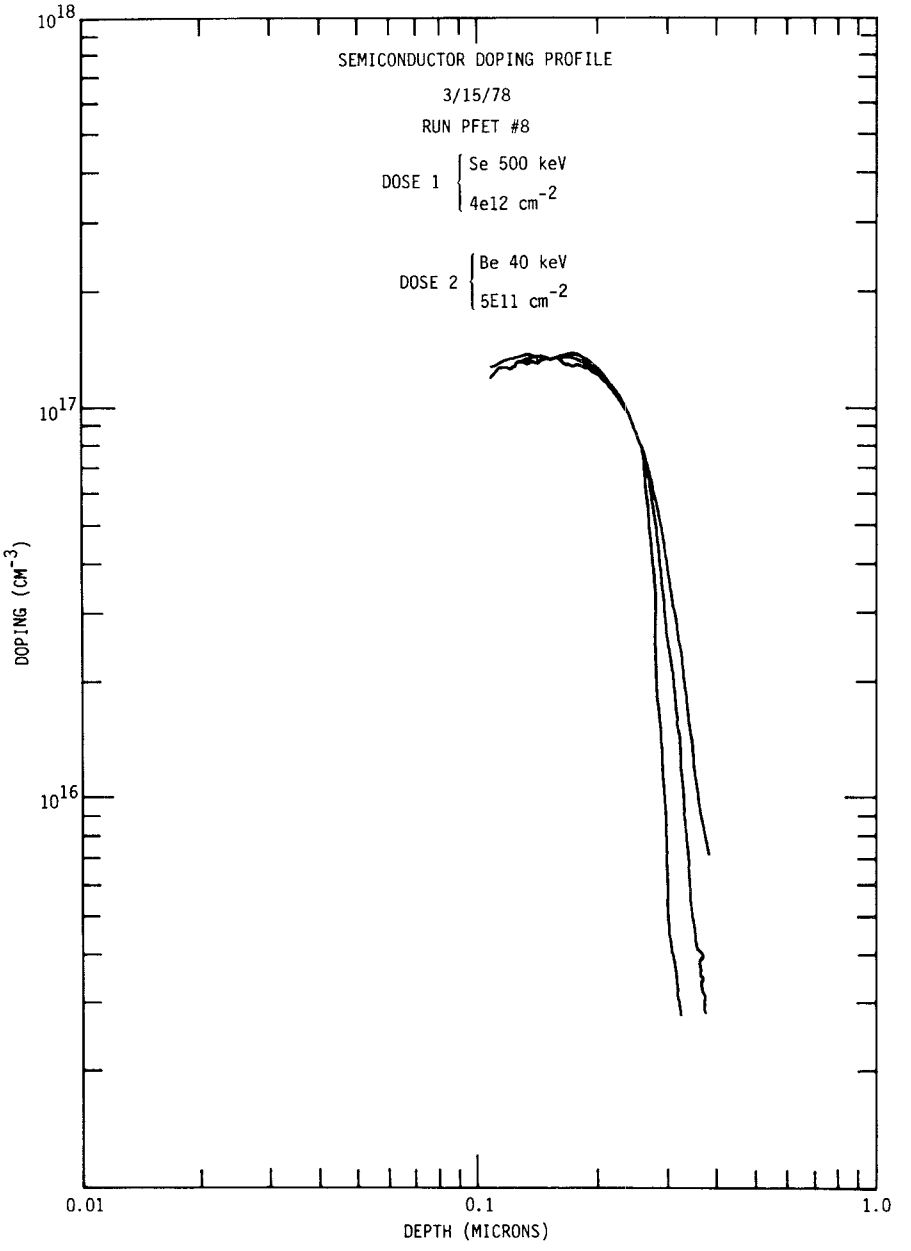

Fig. 6. Measured doping profile for combined 500 keV Se (4×10^{12} cm^{-2}) and 40 keV Be (0.5×10^{12} cm^{-2}) implants.

rise with a drop in drain bias, both at the low input power end and at moderately high input power levels. A more pronounced cancellation notch is noted at the lower drain bias because of the increase in the IMD products due to G_d. It is interesting to note that these results also correspond quite closely to experimentally observed results in Section IV.

As a final note on the calculations, it must be said that the use of a constant load resistance of low value constitutes a useful comparison of the profiles as it serves to simulate large-signal tuning conditions (i.e., optimized tuning for maximum output power) and it also serves to make one other point. By reducing the drain side distortion at lower and intermediate power levels, it accentuates the onset of gate side distortion which sets the maximum power available. This is shown in Fig. 4 where the usefulness of tailored profiles is evident.

III. Device Fabrication

The primary goal of this development program was to realize highly linear GaAs power FET's by tailoring of ion implanted profiles to optimize the doping in the active layer. Therefore, the major development effort in the area of device fabrication was devoted to preparation of suitable active layers. The resulting profiles are presented in this section.

Standard processing techniques were used in completing the fabrication of the transistors; these will be briefly reviewed for completeness.

A. Ion Implantation Profiles

The theoretical calculation in Section II indicated that surface compensated Se+Be implants can provide suitable layers for power FET's with good linearity. Active

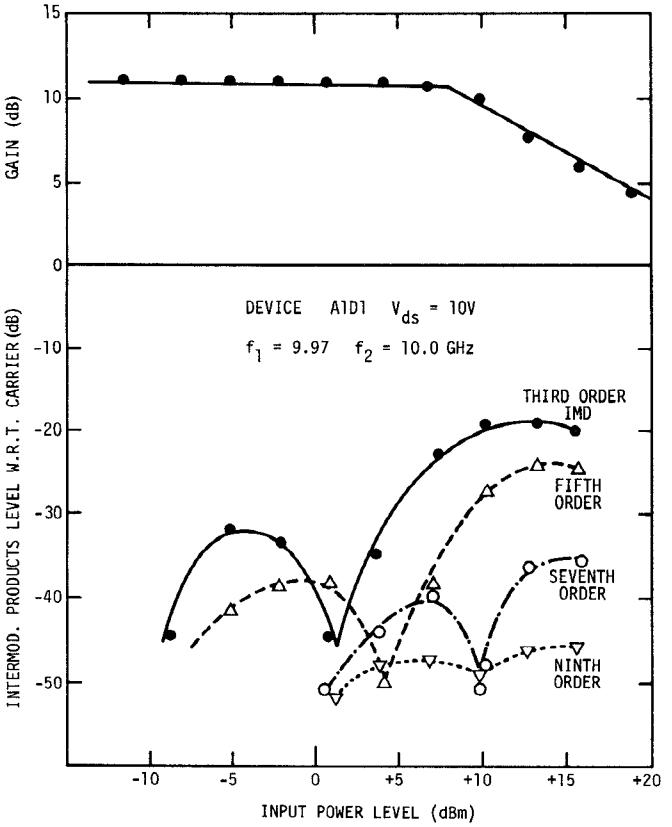

Fig. 7. Measured gain and intermodulation products versus input power for Se implanted GaAs FET at 10 GHz showing evidence of correlated sources on nonlinearity.

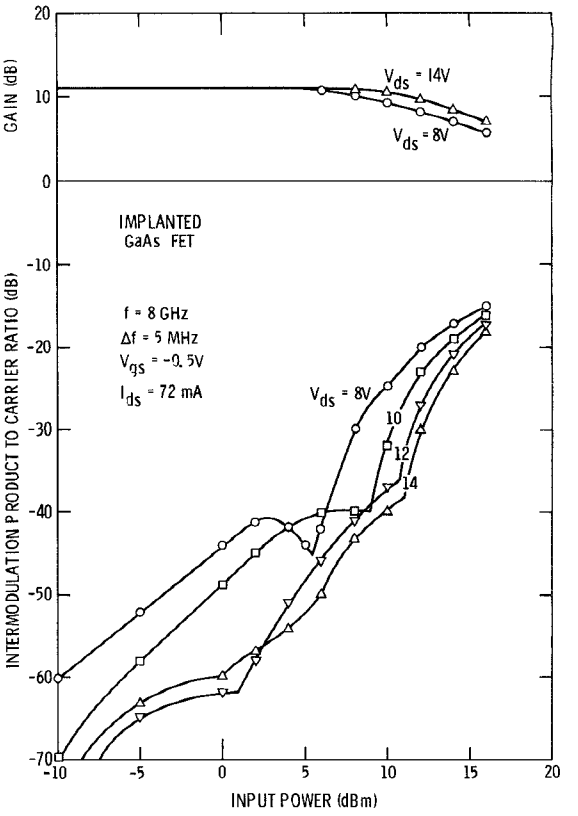

Fig. 8. Measured gain and third-order intermodulation product versus input power for Se + Be implanted GaAs FET at 8 GHz with the drain voltage as a parameter.

layers for experimental measurement of IMD were made from both single dose Se implants and from the combined Se + Be implant scheme of Section II.

A typical profile resulting from such a combined implant schedule is illustrated in Fig. 6. The compensation level in this implant is relatively modest in that the doses of the Se and Be implants were 4×10^{12} and 0.5×10^{12} cm^{-2}, respectively. The pinchoff voltage of such layers is generally about 6 V and from calculations, one may deduce a carrier concentration at the surface region of about 3×10^{16} cm^{-3}.

B. Device Mask and Processing

The unit transistor cell consists of 6 gate fingers which are nominally 1 μm long and 150 μm wide for a total cell periphery of 900 μm. The source-to-drain spacing is 5 μm. The device geometry including the 1-μm long gate structures are defined by conventional photolithographic techniques. The mask set also contains diagnostic patterns for determining ohmic contact resistance, gate metal resistance, doping profile, and mobility.

IV. Intermodulation Measurements

The IMD of the developed transistors has been measured by using the two-tone method. The outputs of two separate signal sources offset by a few MHz are combined in a 3-dB hybrid and are adjusted to equal incident power to the FET. A level set attenuator is used to vary the RF input power, which is read by a power meter. A circulator terminated in a crystal detector is used to monitor the input match. The test circuit consists of coaxial double-slug input-output tuners, which are integrated with the heat sink for the transistor. The total insertion loss of the test circuit is less than 1 dB at 10 GHz. A power meter and a spectrum analyzer are connected to the output of the test circuit to monitor gain, output power, and the intermodulation products.

The level of the sidetones relative to the carrier measured at 10 GHz as functions of the input power are shown in Fig. 7, along with the gain saturation curve for a single dose Se implanted transistor (A1D1, 3×10^{12} cm^{-2} Se ions at 400 keV) operated at a drain voltage of 10 V. The input and output circuits were tuned for maximum output power. The tuning conditions of this transistor show strong correlation effects as evidenced by the dips in the IMD levels.

Improved linearity can be achieved by increasing the drain voltage, as discussed in Section II. In addition, this condition will permit larger RF signals before clipping of the output waveforms. The variation of the third-order intermodulation product as a function of input power level and drain voltage is shown in Fig. 8 for an ion implanted transistor with an improved profile (A7D1, 4×10^{12} cm^{-2} Se ions at 500 keV and 0.5×10^{12} cm^{-2} Be ions at 40 keV). The transistor was tuned for optimum output power which resulted in a small-signal gain of 11 dB at 8 GHz. The large-signal gain is about 2.5 dB higher for a drain voltage of 14 V compared to 8 V, which essentially reflects the ratio of the applied bias powers. The similarity to Fig. 5 is striking.

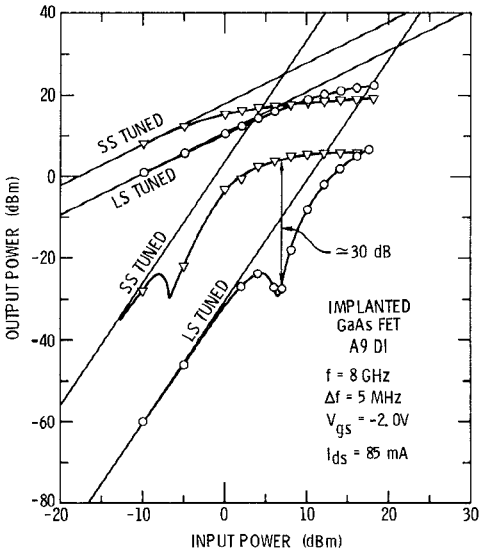

Fig. 9. Measured output power and third-order intermodulation product versus input power for Se implanted GaAs FET at 8 GHz for tuning conditions of maximum linear gain and maximum output power.

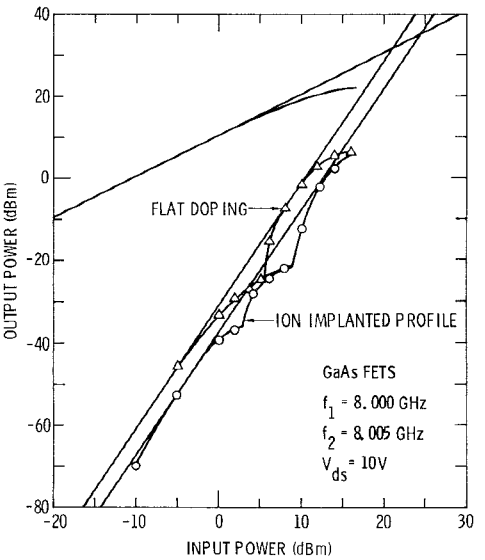

Fig. 10. Comparison of measured output power and third-order intermodulation products versus input power at 8 GHz for conventional epitaxial FET with flat doing and Se+Be implanted FET.

The maximum small-signal gains of the power transistors are substantially higher than the corresponding linear gains when the FET's are tuned for maximum output power. This observation reflects the fact that optimum loading and tuning conditions for an FET are dependent on the signal level, as discussed in Section II. The effects, on the intermodulation products, of tuning to maximum small-signal gains are illustrated in Fig. 9. The maximum small-signal gain is about 18 dB compared to a linear gain of 11 dB for the power tuned case, while the corresponding intercept points are 25 dBm and 32 dBm, respectively. These data illustrate that considerable improvement in the linearity is obtained by tuning the transistor for maximum output power. As an example, it is seen from Fig. 9 that the third-order intermodulation product at the crossover point for the power gain (that point where output power and gain are equal for both tuning conditions) is about 30 dB lower in the power tuned case.

Similar data have been obtained for transistors fabricated on VPE material with flat doping profiles. Again, a substantial reduction was found in the third-order intermodulation product by tuning for output power rather than small-signal gain. Further reduction in the intermodulation distortion could be obtained for these transistors by sacrificing linear gain and large-signal output power.

This compromise of maximum output power in order to obtain minimum IMD was unnecessary with the ion implanted transistors. This observation leads to the important conclusion that the tuning conditions for optimum output power and minimum IMD are virtually identical for optimized profiles (i.e., ion implanted Se+Be profiles) in contrast to conventional transistors with flat doping profiles. Gain is always compromised when tuning for best output power and IMD.

A quantitative measure of the distortion advantage due to the improved tuning and transconductance characteristics of transistors with optimized doping profile is provided in Fig. 10. Here, the third-order intermodulation products have been compared for an ion implanted FET and a transistor with flat doping profile. It is found that the third-order intermodulation product for the implanted FET is significantly lower than for the flat profile VPE transistor. As a result, the third-order intercept point is 4 dB higher for the optimized profile compared to the flat profile. This improvement results in a 2 dB higher power level at a given IMD level for the improved implanted transistor.

These results provide strong evidence for the desirable properties of ion implanted power FET's with optimized doping profiles. The following benefits have been established.

1) The tuning conditions for optimum output power and minimum IMD are virtually identical.
2) As a result of this property, the intercept point for the third-order intermodulation product is several dB higher for an optimized ion implanted profile compared to a conventional flat profile transistor.

The potential of the implanted Se+Be transistors as a power source was evaluated by measuring the output power at 7 GHz with a single-frequency input. An output power of 0.5 W/mm was measured at a drain voltage of 15 V. The associated gain was 5 dB.

V. Conclusions

It has been demonstrated both theoretically and practically that performance advantages can be obtained from tailoring of the active layer profile of a GaAs FET. The importance of optimizing the active layer was highlighted by measuring the IMD levels of a conventional flat profile transistor and an ion implanted device. The more favorable doping profile of the implanted FET resulted in an average reduction of about 6 dB in the third-order IMD

power levels. The results of the present program also indicated that reduced IMD levels can be obtained by increasing the drain voltage beyond the bias point for maximum efficiency. It is also evident from the theoretical and experimental work that the use of an improved profile such as the implanted profile provides a smaller amount of detuning at large-signal levels and makes the maximum power output tuning condition coincide with the test tuning conditions for low IMD levels. This observation provides the power amplifier designer with a considerable advantage.

The methods used to achieve profile tailoring in the present program involved implantation of Se and Be to effect a more advantageous profile. These methods produced the desired effect, as discussed above, and proved the principle involved in lowering IMD.

The theory of IMD distortion developed in this work has furnished explanations for the observed IMD behavior of GaAs FET's which is quite irregular in nature. Further work along these lines are expected to provide the necessary guidelines for obtaining transistors with optimum doping profiles.

Appendix

This Appendix briefly indicates the main calculation steps in determining the IMD ratio in an amplifier, assuming the two contributing IMD sources are the transconductance and the drain conductance.

Let the RF drive voltage impressed upon the gate be a dual tone signal, i.e.,

$$V_g = A[\sin(\omega_1 t) + \sin(\omega_2 t)]. \tag{A1}$$

The RF drain current is given by the transconductance G_m and the expression

$$I_d(t) = \int_0^{V_g(t)} G_m(V_g)\, dV_g. \tag{A2}$$

The third-order intermodulation products may be extracted immediately from this expression; these will be the IMD in the drain current due to the nonlinearities of the transconductance. Table V gives these products directly for the IMD at frequency $2f_1 - f_2$

$$|I|_{(2f_1-f_2)} = 0.25 G_{m3} A^3 + 0.625 G_{m5} A^5. \tag{A3}$$

The drain current of the signal at frequency f_1 is given by

$$I_{f_1} = |G_{m1} \cdot A| \exp(i 2\pi f_1 \tau) \tag{A4}$$

where G_{m1} is the first and dominant term in the polynomial describing transconductance, and τ is the time delay of the gate. Therefore, the ratio of gate-side IMD to signal current is

$$\frac{|I'|_{2f_1-f_2}}{|I_{f_1}|} = \frac{0.25 G_{m3} A^3 + 0.625 G_{m5} A^5}{|G_{m1} A|}. \tag{A5}$$

The drain conductance $G_d(V)$ contributions to the IMD must be calculated by first obtaining V_d the RF drain voltage at the frequency f_1. This is

$$V_d = \frac{I_{f1}}{Y_L} \tag{A6}$$

where Y_L is the load admittance presented to the drain and may be complex. From a knowledge of V_d, a further contribution of IMD current I'' at frequency $2f_1 - f_2$ will be generated, the magnitude of which is given by

$$|I''|_{(2f_1-f_2)} = 0.25 G_{d3} |V_d^3| + 0.625 G_{d5} |V_d|^5 \tag{A7}$$

and the phase of which is determined by the drain load.

Now the total IMD current at frequency $I(2f_1 - f_2)$ will be given by the sum of the two complex currents

$$I_{(2f_1-f_2)} = I'_{(2f_1-f_2)} + I''_{(2f_1-f_2)}. \tag{A8}$$

The ratio of total IMD current to signal current in the load is now obtained simply and translated to power differences in decibels.

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